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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/631,628 | 08/04/2000 | Takeshi Kato | 501.38834X00 | 2314 |

20457 7590 10/27/2003

ANTONELLI, TERRY, STOUT & KRAUS, LLP
1300 NORTH SEVENTEENTH STREET
SUITE 1800
ARLINGTON, VA 22209-9889

| EXAMINER | |
|---|---|
| ROSSOSHEK, YELENA | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2825 | |

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. 09/631,628 | Applicant(s) KATO ET AL. | |
|---|---|---|---|
| | Examiner Helen B Rossoshek | Art Unit 2825 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 August 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-4,7,9-23 and 28-30* is/are rejected.

7)☒ Claim(s) *5,6, 8 and 24-27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 August 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

1. Claims 2, 5, 6, 8, 16, 17, 24, 26 and 28 are objected to because of the following informalities:

Claims 2, 5, 6, 8, 16, 26 and 28 have an insufficient antecedent basis issue.

Claim 17 line 3 delete "angles" insert –angle—

Claim 24 phrase "its control unit" needs to be clarified (which control unit is being referenced)

Claim 24 line 8 after "cache" insert –memory—

Claim 27 line 2 after "supply" insert –control circuit--

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 7, 16, 17, 19, 20 and 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Fu et al. (US Patent 6,633,945).

As to claims 1-4, 7, 16, 17, 19, 20 and 21 Fu et al. teaches an on-chip multiprocessor having multiple independently operable processors mounted in an

integrated circuit chip, wherein at least one pair of processors among the processors are positioned symmetrically relative to each other with respect to a given linear axis or a given origin in the plane of the chip as shown on the Fig. 12 wherein the plurality of independent processors (CP0-CP15) are mounted symmetrically relative to each other with the center point of crossing errors (sharing FCU-MCU and their portions) with equal distances between the processors; an on-chip multiprocessor having multiple independently operable processors mounted in an integrated circuit chip, wherein at least one pair of processors among the processors are positioned symmetrically relative to each other with respect to a given linear axis or a given origin in the plane of the chip and a controller for the pair of processors is located in the area containing the linear axis or origin as shown on the Fig. 12, wherein FCU-MCU (flow control unit with memory control) are in the area of the center point of the layout; an on-chip multiprocessor having multiple independently operable processors mounted in an integrated circuit chip, wherein at least one pair of processors among the processors are positioned symmetrically relative to each other with respect to a given linear axis or a given origin in the plane of the chip; delays in transmission between the multiprocessor controller and each processor of the pair of processors are almost equal; and the shared portions connected through the controller to the pair of processors are located in the area containing the linear axis or origin within the symmetric multiprocessor system based on the fully connected multiple FCU architecture reduces the memory read latencies and increases bandwidth between processors and shared memory (col. 2, ll.1-7; col. 3, ll.14-20); an on-chip multiprocessor having multiple

independently operable processors mounted in an integrated circuit chip, wherein: some of the logical units or cache memories constituting each processor are dual and redundant; in at least one pair of processors, two logical units or cache memories with the same function as a pair are symmetric relative to each other with respect to a given first linear axis in the chip plane; the controller for the pair of processors is located in the area containing the first linear axis; the distances from the controller to both the processors are almost equal; and two logical units or cache memories as a dual unit included in each processor are symmetric relative to each other with respect to a given second linear axis (col. 3, ll.12-20); the first linear axis and second linear axis intersect at right angle as shown on the Fig. 12; the first linear axis (vertical) is perpendicular to the direction of data flow in the logical units and the second linear axis (horizontal) is parallel to the direction of data flow as shown on the Fig.12; the pair of processors also have cache memory shared by them, and storage control unit for controlling processing of signals between the shared cache memory and the pair of processors; and the shared cache memory and storage control unit are located in the area by using flow control unit (FCU) shown on the Fig. 12 (col. 1, ll.52-55); the pair of processors also share I/O circuit group, and storage control unit for controlling signal transmission between the I/O circuit group and the pair of processors is located in the area (col. 2, ll.65-67; col. 3, ll.1-8).

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 9-11, 15, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. as applied to claim 1 above, and further in view of Shimizu et al. (5,787,310).

As to claims 9-11, 15, 22 and 28 Fu et al. teaches the features outline previously, but lacks specifics regarding the structure of the processor. However Shimizu et al. teaches the processors have logical units and cache memories as shown on the Fig. 24; the logical units and cache memories have each logical blocks and memory mats as shown on the Fig. 26, Fig. 47; a clock generator, which supplies clock signals in common or separately to the controller and the shared portions, is located in the area as shown on the Fig. 52 describing the example 37 (col. 14, ll.29-31); a I/O pins of the processors consist of bump arrays and the arrangement of bumps on the surfaces of the pair of processors is symmetric with respect to the linear axis or origin as shown on the Fig. 52 (col. 14, ll.21-28); the pair of processors are symmetric with respect to a linear axis parallel or perpendicular to the direction of data flow in the logical units, or point-symmetric (180° rotation) with respect to the origin as shown on the Fig. 24. It would have been obvious to one of ordinary skills in the art at the time the invention was made to have used Shimizu et al. to teach specifics subject matter Fu et l. does not teach, because the configuration is such that a space is provided between the memory cell region tows and the processor is arranged in the space, so other processors can be

arranged in the space to configure multiprocessor, where the bus interface is provided at the signal output terminal, each signal can be outputted at a high speed.

6. Claims 12 and13 rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. in view of Shimizu et al. as applied to claim 9 above, and further in view of Gilmer et al. (US Patent 5,998,270).

As to claims 12 and 13 the combination of Fu et al. in view of Shimizu et al. teaches the features outline previously, but lacks specifics regarding consisting of the logical circuit groups and memory circuit groups. However Gilmer et al. teaches the logical circuit groups and memory circuit groups consist of MOS transistor circuits, and sources, gates and drains inside the circuit groups or p-MOS and n-MOS transistors as shown on the Fig. 1 wherein the MOS semiconductor device is depicted and MOS transistor (typically is symmetrical) formed on the semiconductor substrate and having gates (col. 1, ll.21-24; ll.29-32); at least some of the MOS transistors in the pair of processors have one gate and a source and drain at one side of the gate, a drain and source, opposite to the source and drain, at the other side of the gate, and also have two gates through which a same signal is inputted, one drain between the gates, and two sources outside the gates (col. 1, ll.32-36; ll.48-57); It would have been obvious to one of ordinary skills in the art at the time the invention was made to have used Gilmer et al. to teach specifics subject matter the combination of Fu et al. in view of Shimizu et al. does not teach, because when the substrate-oxynitride layer interface is used to form a gate oxide-substrate interface, device performance can be improved by improving leakage current characteristics and reducing hot carrier degradation.

7. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. as applied to claim 1 above, and further in view of Satoh et al

As to claim 14 Fu et al. teaches the features outline previously, but lacks specifics regarding the processor comprising MOS transistor circuits. However Satoh et al. teaches the processors comprise MOS transistor circuits (col. 4, ll.25-27). It would have been obvious to one of ordinary skills in the art at the time the invention was made to have used Satoh et al. to teach specifics subject matter Fu et l. does not teach, because it can be applied to high speed digital processors consisting of exclusive integrated circuits and various other digital units and apparatus consisting of bipolar gate array integrated circuit (col. 14, ll.11-14).

8. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. as applied to claim 16 above, and further in view of Tobita (US Patent 5,646,516).

As to claim 18 Fu et al. teaches the features outline previously, but lacks specifics regarding MOS transistors orientation. However Tobita teaches the processors comprise MOS transistor circuits, and the first linear axis (Y) is parallel to the MOS transistor gate width direction and the second linear axis (X) is parallel to the MOS transistor gate length direction as shown on the Fig. 2A wherein W is the width and L is the length (col. 8, ll.45-49). It would have been obvious to one of ordinary skills in the art at the time the invention was made to have used Tobita to teach specifics subject matter Fu et l. does not teach, because a circuit which employs MOS transistors is formed, so that a stable reference voltage can be generated with significantly reduced

dependency upon power temperature and no dependency upon supply voltage (col. 38, ll.12-17).

9. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. as applied to claim 4 above, and further in view of DeFlon et al. (US Patent 5,742,180).

As to claim 23 Fu et al. teaches the features outline previously, but lacks specifics regarding power supply of the processors. However DeFlon et al. teaches a power supply control circuit, which supplies electric power in common or separately to the pair of processors, the controller and the shared portions, is located in the area within DPGA (processor) (col. 1, ll.12, ll.63-67; col. 13, ll.1-6) shown on the Fig. 2A (col. 6, ll.32-36) and providing it with the power and ground (col. 13, ll.31-37). It would have been obvious to one of ordinary skills in the art at the time the invention was made to have used DeFlon et al. to teach specifics subject matter Fu et l. does not teach, because the logic elements include locally stored multiple contexts dictating different combinatorial logic operations performed by the logic elements, the context increase the logic operations performance by the logic element and the fact that the context are locally stored enables better integration and speed (col. 3, ll.55-60).

10. Claims 29 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fu et al. as applied to claim 1 above, and further in view of Lee et al. (US Patent 5,585,210).

As to claims 29 and 30 Fu et al. teaches the features outline previously, but lacks specifics regarding the manufacturing using separate semiconductor mask pattern and

wiring pattern for different portions of the semiconductor. However Lee et al. teaches one processor on the pair of processors is manufactured using semiconductor mask pattern 1 and the other is manufactured using semiconductor mask pattern 2 as shown on the Fig. 1 wherein mask pattern (P1) is for forming one portion of the semiconductor and mask pattern (P2) is for forming different portion of the semiconductor (col. 1, ll.54-56); wiring pattern 1 for one processor in the pair of processors and wiring pattern 2 for the other processor as shown on the Fig. 1 wherein mask pattern (P3) is for forming the wiring between two regions on the semiconductor (col. 1, ll.56-57). It would have been obvious to one of ordinary skills in the art at the time the invention was made to have used Lee et al. to teach specifics subject matter Fu et I. does not teach, because the additional pattern may be positioned in the crossing spaces of the matrix pattern and connected to the edges of the matrix pattern or may be inserted into spaces and using the supplemental line-type additional pattern among the various modifications could be provided in the spaces of the matrix pattern along the X axis and Y axis (col. 4, ll.45-55).

***Allowable Subject Matter***

11. Claims 5, 6 and 8 contain allowable subject matter. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach at least one pair of processors among the processors are situated at positions shifted from positions symmetric with respect to a given linear axis or given origin in the plane of the chip: in direction parallel to the axis or the centerline of the area of the pair; in a direction parallel to the axis or the centerline of the area of the pair; and the controller for the pair of processors is located in the area containing the

linear axis or origin; delays in transmission between the controller and each processor of the pair of processors are almost equal; and the shared portions connected through the controller to the pair of processors are located in the area containing the linear axis or origin.

12. Claims 24-27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter: the prior art of record does not teach each of the processors has first cache memory and a first cache memory control unit for controlling it; in the pair of processors, the first cache control units are located beside one side of each processor area nearer to the linear axis or origin; and the lower level cache control unit is located between the first cache memory control units as a pair; each of the processors has a first control unit for controlling its input/output signals; multiple processors share I/O circuit group through a second control unit; in the pair of processors, the first control units are located beside one side of each processor area nearer to the linear axis or origin; and the second control unit is located between the first control units as a pair; a pattern of clock trees which distribute clock signals to the pair of processors is symmetric with respect to the linear axis or origin; the pattern of power supply wiring control circuit which supplies electric power to the pair of processors is symmetric with respect to the linear axis or origin.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen B Rossoshek whose telephone number is 703-305-3827. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 703-308-1323. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

HR HR

A. M. THOMPSON
MASTER'S LEVEL PATENT EXAMINER
TECHNOLOGY CENTER 2800